IN THE CLAIMS

Please amend the claims as follows:

1.   1.   (currently amended) A differential amplifier circuit comprising:

2   a first differential amplifier for receiving a pair of differential input signals to
3   generate a first output;

4   a second differential amplifier for receiving said pair of differential input signals
5   to generate a second output; ~~and~~

6   a summing circuit for summing said first output of said first differential amplifier
7   and said second output of said second differential amplifier to provide a common output
8   for said differential amplifier circuit; and

9   a reference voltage generation circuit for providing a reference voltage signal to
10   said summing circuit, wherein said reference voltage generation circuit is a differential
11   amplifier.

1.   2.   (original) The differential amplifier circuit of Claim 1, wherein said first differential
2   amplifier is an n-channel differential amplifier.

1.   3.   (original) The differential amplifier circuit of Claim 2, wherein said first differential
2   amplifier includes a pair of n-channel transistors for receiving said pair of differential input
3   signals, respectively.

1.   4.   (original) The differential amplifier circuit of Claim 1, wherein said second differential
2   amplifier is a p-channel differential amplifier.

1   5.   (original) The differential amplifier circuit of Claim 1, wherein said second differential
2   amplifier includes a pair of p-channel transistors for receiving said pair of differential input
3   signals, respectively.

1   6.   (original) The differential amplifier circuit of Claim 1, wherein said summing circuit is
2   an n-channel differential amplifier.

1   7.   (currently amended) The differential amplifier circuit of Claim ~~6~~ 1, wherein said summing
2   circuit includes a~~n~~ ~~pair of~~ n-channel transistors ~~for receiving~~ pair, wherein a first transistor of said
3   n-channel transistor pair receives said voltage reference signal from said reference voltage
4   generation circuit, wherein a second transistor of said n-channel transistor pair receives combined
5   ~~and~~ output signals from said first output of said first differential amplifier and said second output
6   of said second differential amplifier.

1   8.   (currently amended) The differential amplifier circuit of Claim ~~7~~ 1, wherein said reference
2   voltage generation circuit is a p-channel differential amplifier ~~circuit further includes a reference~~
3   ~~voltage generation circuit for providing said reference voltage for said summing circuit.~~

1   9.   (currently amended) The differential amplifier circuit of Claim 8, wherein said reference
2   voltage ~~reference~~ generation circuit receives an active low ENABLE_P signal ~~includes a~~
3   ~~differential amplifier having inputs connected to an output of said differential amplifier.~~

1   10.   (original) The differential amplifier circuit of Claim 1, wherein said first and second
2   differential amplifiers receive an active low ENABLE_N signal.

1   11.   (original) The differential amplifier circuit of Claim 10, wherein said summing circuit
2   receives an active low ENABLE_P signal.

1   12.   (original) The differential amplifier circuit of Claim 11, wherein said summing circuit
2   includes a clamp device to hold said common output high when said ENABLE_P signal is low.

1   13.   (original) The differential amplifier circuit of Claim 1, wherein said first differential
2   amplifier receives a gate control voltage V_{CMN} to control the current through an n-channel
3   transistor within said first differential amplifier in a consistent and predictable manner using a
4   current mirror technique.

1   14.   (original) The differential amplifier circuit of Claim 1, wherein said second differential
2   amplifier receives a gate control voltage V_{CMP} to control the current through a p-channel transistor
3   within said second differential amplifier in a consistent and predictable manner using a current
4 .   mirror technique.

1   15.   (original) The differential amplifier circuit of Claim 1, wherein said summing circuit
2   receives a gate control voltage V_{CMN} to control the current through an n-channel transistor within
3   said summing circuit in a consistent and predictable manner using a current mirror technique.